(12) UK Patent Application (19) GB (11) 2 097 206 A

(21) Application No 8112357
(22) Date of filing
21 Apr 1981
(43) Application published
27 Oct 1982
(51) INT CL³ H03L 7/18
(52) Domestic classification
H3A L2D2 L3X L4 LX P QA T
(56) Documents cited
GB A 2026268
GB A 2015277
GB 1515066
"Frequency domain yields its data to phase Pocket Synthesizer" By J G Gibbs & R Temple in "Electronics' Journal of April 27 1978 see pages 107–113
(58) Field of search
H3A
H4P
(71) Applicant
The Marconi Company Limited
Marconi House
New Street
Chelmsford
Essex CM1 1PL
(72) Inventor
Boleslaw Marian Sosin
(74) Agents
C F Hoste
Marconi House
New Street
Chelmsford
Essex CM1 1PL

(54) Frequency synthesisers

(57) In a phase lock loop type frequency synthesiser including a dual, modulus, switched frequency divider positioned between the variable oscillator and the phase comparator, to allow a relatively high reference frequency to be used, whilst permitting fine frequency resolution to be achieved for the output frequency. A compensation signal is generated in step with the integral change of divisor value, and the effect of the compensation signal on the feedback loop signal subject to phase jitter arising the divider switching process is monitored. The magnitude of the compensation signal is adaptively adjusted to reduce phase jitter to a minimum. The gain of a digital-to-analogue converter, which receives as an input a digital value which is directly related to the variation in the integral division ratio or the gain of the phase comparator or of an attenuator between the converter and the phase comparator may be adjusted. The converter 9 output may alternatively control a loop phase shifter 24.

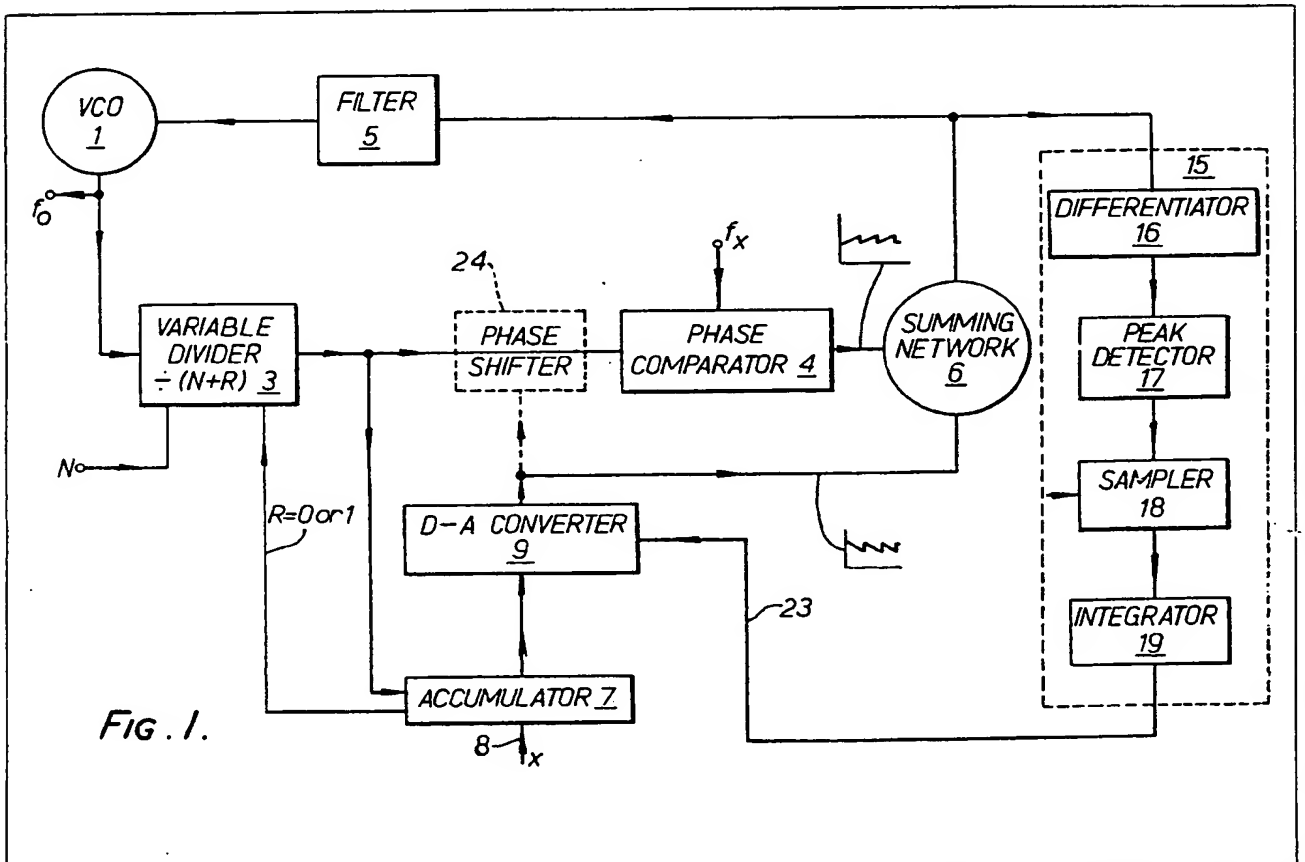

FIG. 1.

GB 2 097 206 A

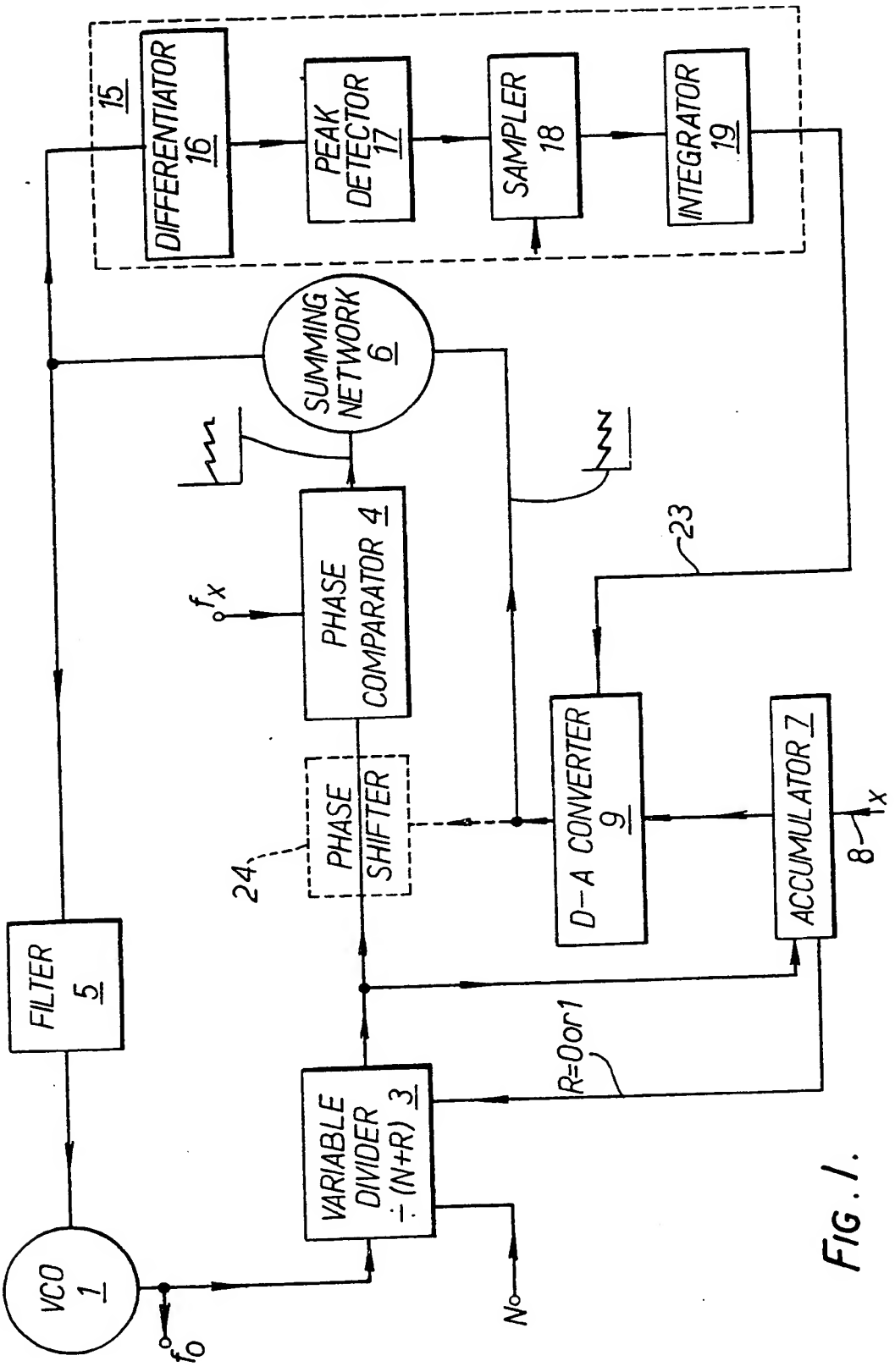
15
DIFFERENTIATOR 16
PEAK DETECTOR 17
SAMPLER 18
INTEGRATOR 19
SUMMING NETWORK 6
PHASE COMPARATOR 4
f_x
23
PHASE SHIFTER
24
D-A CONVERTER 9
ACCUMULATOR 7
8
x
FILTER 5
R=0or1
VARIABLE DIVIDER ÷(N+R) 3
VCO 1
f_o
N_o

FIG. 1.

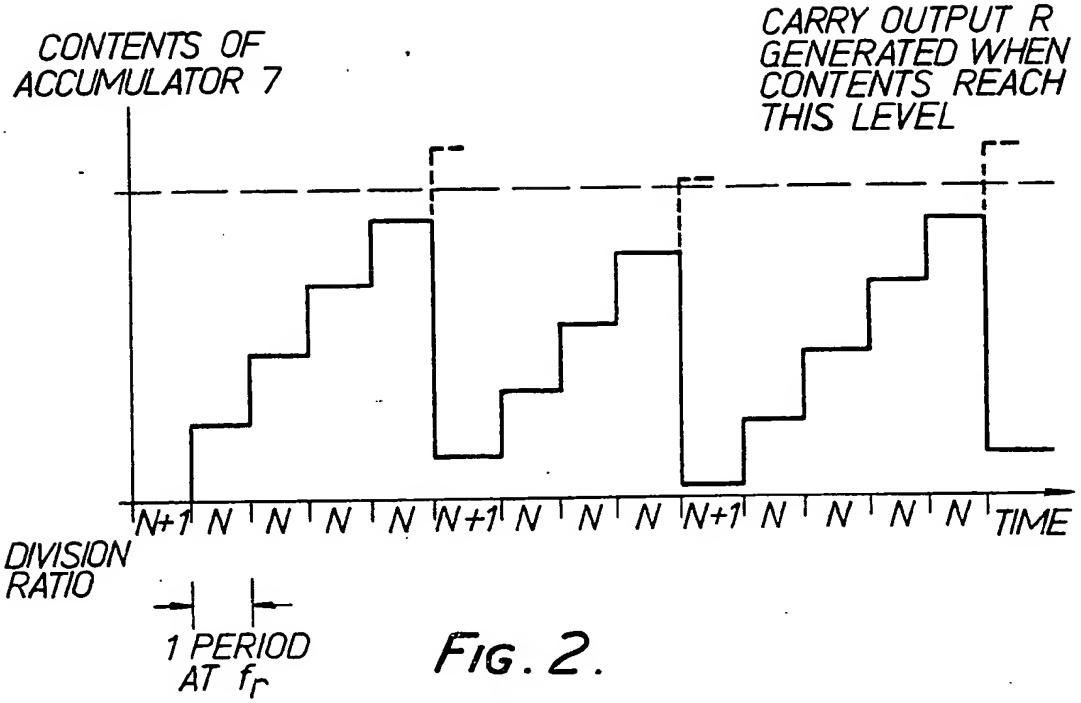

FIG. 2.

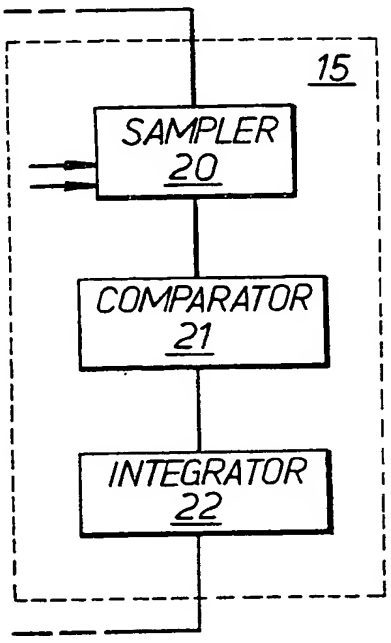

FIG. 3.

SPECIFICATION

Frequency Synthesisers

This invention relates to frequency synthesisers. A frequency synthesiser is capable of generating an output frequency with an accuracy which is determined by that of a stable frequency reference source. Often a variable frequency oscillator is coupled to the reference source by means of a phase lock loop in which the output frequency f_o is related to the reference frequency f_r by the relationship $f_o = N.f_r$, where N is a divisor by which the output frequency is divided before it is compared with the reference value. Conveniently, the factor N is produced at a frequency divider and it is clear that if N is an integer, the smallest increment in output frequency value is necessarily equal to the magnitude of the reference frequency f_r itself. This means that for frequency synthesisers requiring fine resolution between its different possible output frequencies, a very low value reference frequency is needed, but this in turn requires a long setting time constant for the phase lock loop.

It has been proposed to overcome this difficulty by using various expedients, particularly involving the use of a number of individual phase locked loops which are inter-related with each other, but these cause spectrally impure output signals which are unsatisfactory for many applications. Additionally, the expense and complexity of multi-loop frequency synthesisers is a severe disadvantage.

An alternative solution is to adopt non-integral values of N in the relationship given above so that a relatively high value reference frequency can be used to generate output frequencies of fine resolution, whilst needing only a single phase lock loop to achieve them. Such a technique is often called fractional-N synthesis or sometimes called side step programming. In practice, frequency dividers divide only by integral values, and fractional division is simulated by altering the integral value itself during the course of a division cycle. Thus the non integer division ratios are simulated by dividing by, say, N + 1 instead of N on a proportion x of the cycles giving an average division ratio which approximates closely to N, x where N is the integer portion and x is the fractional portion of the average value: e.g. if the average division ratio is, say 123.45 then N is 123 and x is 0.45. The main disadvantage of this scheme is the phase jitter which is generated on the divider output by changing between two or more different division ratios.

A frequency synthesiser which uses the last mentioned technique and which additionally reduces the phase jitter to a significant extent is described in out earlier U.K. patent 1,560,233. Even so, the phase jitter may not be completely removed and the present invention seeks to provide a frequency synthesiser in which this disadvantage is reduced.

According to this invention, a frequency synthesiser includes a controllable oscillator, a frequency divider and a phase comparator in a feedback loop arranged to control the oscillator by means of a control signal to a frequency which is related to a reference frequency by the divisor, said divisor includes, or consists of, a controllable integral factor which is changed periodically by an integer when the accumulated sum of a periodically occurring first quantity amounts to, or exceeds, a predetermined second quantity, so as to produce, in effect, a non intergral relation between the oscillator frequency and the reference frequency; means for deriving from said sum as it is accumulated a jitter compensation signal which is used to suppress phase jitter in the oscillator control signal that would otherwise result from periodic changes of said integral factor; and monitoring means for monitoring the extent of said suppression and for modifying the magnitude of the jitter compensation signal in response thereto so as to minimise the phase jitter.

The invention is further described by way of example with reference to the accompanying drawings, in which

Figure 1 is a block diagram of the synthesiser in accordance with this invention.

Figure 2 is an explanatory diagram, and

Figure 3 shows an alternative form of part of Fig. 1.

Referring to Fig. 1, the frequency synthesiser includes a voltage controlled oscillator 1, a frequency divider 3 and a phase comparator 4 the outpt of which is applied to control the VCO1 by way of a low pass loop filter 5. A sinusoidal output signal of frequency f_o is derived from the VCO1. Zero crossings, or other cycle markers, are counted by the variable divider 3 which gives one output pulse for every N input cycles. The integral dividing factor N is, however, controllable according to an external input value.

The phase comparator 4 gives an output which varies with the phase difference between the divider output and the reference frequency and will require to be filtered by the loop filter 5 to maintain stability of operation. For this reason the bandwidth of the filter 5 must be restricted in relation to the reference frequency f_r.

In order to obtain in effect a non integral divisor value, the dividing factor, normally N, is periodically increased to N + 1 for a fraction x of the time. This technique alone tends to introduce phase jitter in the loop as a result of the periodic programmable divider. In Fig. 1, this jitter is avoided by, in effect, subtracting out the step change in the error output from the comparator 4 that would otherwise arise over the period of that step

change. This is achieved by adding into the output of the comparator 4 by way of a summing network 6 a voltage which represents the continuously increasing phase error in the pulse train output from the variable divider 3. The result is that the VCO1 receives a steady control signal and produces a jitterless output signal f_o, while there is still a step change in the divider output phase.

This compensation voltage is derived as follows. An accumulator 7 adds at every output pulse from the divider 3, i.e. at the reference frequency, a number x present on line 8 to the previously accumulated sum already held in the accumulator 7. When the accumulator is filled completely a carry bit R is generated and is used to increase the dividing factor of divider 3 by unity, it thus being N + 1. When the carry bit is generated the contents of the accumulator is just that amount by which the previous sum exceeded unity.

Fig. 2 illustrates this process over a period of three such cycles of the dividing factor and the accumulator 7. It can be seen that contents of the accumulator 7 increases in discrete steps, each of which represents the fraction x, until the accumulator overflows and generates a carry bit. It will thus be appreciated that when a carry bit is generated, the contents of the accumulator itself drops sharply and then increases again in the step like fashion.

It is the periodic changes in divisor value which are detected by the phase comparator and emerge as a jitter voltage on the comparator output. This jitter is reduced as follows. In Fig. 1, in addition to the accumulator 7 providing a divider correction to achieve a correct average dividing factor, the accumulated sum shown in Fig. 2 is applied to a digital-to-analogue (D-A) converter 9 at each increment to provide an analogue signal continuously representative of the phase error between the reference frequency pulses and the nearest preceding pulse input to the programmable divider. This analogue signal is of course a reflection of the jitter voltage that appears in the output of the phase comparator since they have a common cause. The D-A output voltage is therefore appropriate, with suitable scaling, for incorporation with the comparator output signal so as to eliminate the jitter voltage. The analogue voltage is therefore applied to the summing network 6. The gain of the D-A converter 9 output should be such that the full scale peak-to-peak voltage from the D-A converter 9 should cancel out the voltage-change on the phase comparator output, produced by a phase shift of 1 cycle at the variable divider input.

In practice, the gain of the converter 9 is critical if complete suppression of the phase jitter at the summing network 6 is to be achieved and in reality the degree of suppression is unlikely to be perfect if the gain is preset to a fixed value. Accordingly, a monitor circuit 15 is provided which monitors the output of the summing network 6 in order to detect the presence of any jitter which would cause undesirable frequency modulation of the frequency of the oscillator 1. If any jitter is detected by the monitor 15, it acts in an adaptive manner to modify the gain of the converter 9 so as to remove it. The monitor 15 receives the output signal from the summing network 6 which is fed to a differentiator 16 forming part of the monitor. Phase jitter is manifest as a periodic abrupt transition in the level of the control signal fed to the oscillator 1 via the filter 5, and consequently the differentiator 16 acts to convert these abrupt transitions in signal spikes. Any signal spikes generated by the differentiator 16 are fed to a peak detector 17, which shapes the signal spikes to remove gross irregularities and to produce a signal having an amplitude corresponding to the maximum amplitude of the spikes. Since it is expected that the signal spikes will occur in the region of phase transitions in the output of the phase comparator 4 the signals generated by the peak detector 17 is sampled within this time window. The sampler 18 is controlled by the accumulator 7 (via a lead not shown) so that the sampler 18 samples the output of the peak detector 17 immediately following a change in the divisor value applied by the accumulator 7 to the variable divider 3. In this way the output of the sampler 18 is only related to phase transistions or jitter assoicated with the changes in the divisor value of the variable divider 3. The sampled signals are integrated over a reasonable time period by means of an integrator 19 having a time constant which is longer than the period of the reference frequency f_r multiplied by the fraction X, ie. longer than the period of the frequency represented by f_r times x. The output of the integrator 19 is indicative of the extent to which the compensation signal generated at the converter 9 differs from the variations in the phase comparator 4. Thus it is an indication of the extent to which the phase jitter is not completely suppressed as ideally the signal fed to the integrator 19 has zero value. Thus when the phase jitter is completely suppressed the input to the integrator 19 will become zero. However, the integrated value held by the integrator is then not zero, but a constant value which is used to modify the gain of the digital-to-analogue converter 9 over lead 23 in such a sense as to minimise the phase jitter.

It will be appreciated that the integrator 19 represents not only the magnitude of the phase jitter present at the output of the summing network 6, but also its polarity. Thus the monitor circuit 15 acts in conjunction with the variable divider 3 to provide a compensation for phase jitter, but the com-

pensation is not a true feedback signal, since the compensation does not occur in real time. Instead the gain of the converter 9 is periodically modified to take into account errors which develop during the immediately preceding monitor periods.

Fig. 3 shows an alternative form that the monitor circuit 15 can take. The modified monitor circuit does not incorporate a differentiating circuit, but instead contains a sampler 20 which is arranged to sample the output signal of the adder 6 immediately before and immediately after the divisor value of the variable divider 3 is altered under the action of the accumulator 7. The two sampled values are compared at a comparator 21 and their difference is integrated at an integrator 22. Clearly if both sample values are equal, no phase jitter is present at the output of the summing network 6 and no correction signal is generated by the integrator 22. However, if the converter 9 does not exactly cancel the phase jitter present at the output of the phase comparator 4, the two sample values will not be equal and the signals generated at the comparator 21 will accumulate within the integration period of the integrator 22. As before the magnitude and polarity of the integrated signal is used to modify the gain of the converter 9, so as to minimise any jitter present at the output of summing network 6.

If desired a further improvement can be made by monitoring at more than the two points which immediately precede and follow the periodic change in divisor value to allow for any average change or gradual shift in level of the control voltage applied to the oscillator 1.

In Fig. 1, it is the variations and transitions in the output of the variable divider 3 which give rise to the phase jitter at the output of the phase comparator 4. The phase jitter is present because the output pulses generated by the variable divider 3 are not regularly spaced at a frequency which corresponds to the reference frequency f_r applied to the second input of the phase comparator 4. In other words, it is the irregularity of occurrence of the output pulses of variable divider 3 which gives rise to the phase jitter at the output of the phase comparator 4, since the reference frequency f_r is completely stable and regular.

In Fig. 1, the compensation signal is applied by the converter 9 so as to modify the output of the phase comparator 4, but this need not necessarily be the case and, instead, the irregularities in the output of the variable divider 3 can be suppressed before the signal is applied to the input of the phase comparator 4. This modification is represented by the presence of the phase shifter 24 which generates a phase delay which is dependent on the changing amplitude of the output of the converter 9. Thus the converter 9 operates directly to provide phase compensation rather than to generate an amplitude compensation signal for application to the summing network 6. When the phase shifter 24 is present the summing network 6 is not used. In some instances it may be preferable to introduce compensation for phase jitter by means of the phase shifter 24 rather than the summing network 6.

It will be appreciated that although the gain correcting information from the integrator 19 or 22 is applied via a line 23 to the A-D converter 9, it could alternatively be applied to the phase comparator 4 to control its effective gain. Alternatively a variable attenuator or a variable gain amplifier placed in the line between the phase comparator 4 and the summing network 6 or the D-A converter 9 and the summing network 6 will be controlled by the line 23.

CLAIMS

1. A frequency synthesiser including (a) a controllable oscillator, (b) a frequency divider, and (c) a phase comparator in a feedback loop arranged to control the oscillator by means of a control signal to a frequency which is related to a reference frequency by the divisor, said divisor includes, or consists of, a controllable integral factor which is changed periodically by an integer when the accumulated sum of a periodically occurring first quantity amounts to, or exceeds, a predetermined second quantity, so as to produce, in effect, a non integral relation between the oscillator frequency and the reference frequency; means for deriving from said sum as it is accumulated a jitter compensation signal which is used to suppress phase jitter in the oscillator control signal that would otherwise result from periodic changes of said integral factor; and monitoring means for monitoring the extent of said suppression and for modifying the magnitude of the jitter compensation signal in response thereto so as to minimise the phase jitter.

2. A frequency synthesiser as claimed in claim 1 and wherein said first quantity occurs once in each period of the reference frequency and the ratio of the first to the second quantities is equal to the fractional average change of said integral factor.

3. A frequency synthesiser as claimed in claim 1 or 2 and wherein the jitter compensation signal is added to the output of the phase comparator to suppress undesired amplitude variations thereof.

4. A frequency synthesiser as claimed in claim 1 or 2 and wherein the jitter compensation signal is used to alter the phase of a signal applied to phase comparator from said frequency divider to suppress undesired phase variations thereof.

5. A frequency synthesiser as claimed in any of the preceding claims, and wherein said monitoring means is adapted to monitor the

control signal present in said feedback loop between the output of said phase comparator and the controllable oscillator.

6. A frequency synthesiser as claimed in claim 5 and wherein the monitored control signal is differentiated to enable signal level transistions to be identified, and the signal level transitions are used to modify the magnitude of the jitter compensation signal.

7. A frequency synthesiser as claimed in claim 6 and wherein a signal derived from the differentiated control signal is sampled immediately following the instant at which said integral factor of the frequency divisor is altered.

8. A frequency synthesiser as claimed in claim 7 and wherein successive samples are integrated over a number of periods of said reference frequency, and the intergrated value is used to modify the magnitude of the jitter compensation signal.

9. A frequency synthesiser as claimed in claim 5 and wherein the monitored control signal is sampled immediately preceding and immediately following the instant at which said integral factor of the frequency divisor is altered.

10. A frequency synthesiser as claimed in claim 9 and wherein the two samples are compared with each other, and any difference in sample level is integrated over a number of periods of said reference frequency, and the integrated value is used to modify the magnitude of the jitter compensation signal.

11. A frequency synthesiser substantially as illustrated in and described with reference to Fig. 1 or Fig. 4 of the accompanying drawings.

Printed for Her Majesty's Stationery Office
by Burgess & Son (Abingdon) Ltd.—1982.
Published at The Patent Office, 25 Southampton Buildings.
London, WC2A 1AY, from which copies may be obtained.